UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/419,386	10/15/99	FOX B	TRI-003

TM02/0518

LESTER J. VINCENT
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES CA 90025

EXAMINER	
BRAGDON, R	
ART UNIT	**PAPER NUMBER**
2185	14

DATE MAILED: 05/18/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/419,386	Applicant(s) FOX ET AL.	
	Examiner Reginald G. Bragdon	Art Unit 2185	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *4-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of invention I, claims 1-3, in Paper No. 13 is acknowledged.

2. Claims 4-13 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention. Election was made **without** traverse in Paper No. 13.

Information Disclosure Statement

3. The information disclosure statements received 10-15-1999 and 11-26-1999 have been considered by the Examiner. See the attached PTO-1449s.

Drawings

4. The drawings have been objected to by the Office Draftsperson under 37 CFR 1.84 or 1.152 as noted in the attached PTO-948.

Specification

5. The status of the application on page 19, lines 2-5, should be updated as appropriate.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Gilson (5,361,373).

As per claim 1, Gilson teaches a Field Programmable Gate Array (FPGA) 12 including a computing device 10 ("configurable system on a chip"). The computing device 10 includes a configuration memory array 20 ("configurable system logic"). A "system bus" is represented by the bus interconnecting the host I/F, configuration memory array, and reconfigurable instruction execution unit. Configuration data is loaded into the configuration memory array 20 over the bus by Host 40 ("configuring a memory cell in the CSL using the system bus"). See column 5, lines 46-50. The configuration data is then utilized tc configure the reconfigurable instruction execution unit ("reading the memory cell in the CSL using the system bus"). See column 7, lines 26-35.

8. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Gittinger et al. (5,668,815).

As per claim 1, Gittinger et al. teaches a microcontroller formed on a single monolithic semiconductor substrate ("configurable system on a chip"). The microcontroller includes a processor core 16 ("CPU"), DMA control 20, a central bus 34 ("system bus") and internal memory 30 ("configurable system logic"). See figure 1. The internal memory 30 is initialized

("configuring a memory cell in the CSL using the system bus") with a selected background pattern. See column 12, lines 40-42. Then the background pattern is read from the memory ("reading the memory cell in the CSL using the system bus"). See column 13, lines 21-23.

As per claim 2, Gittinger et al. teaches that the DMA control 20 controls the initialization and reading of the internal memory data during the test operation. See column 12, lines 40-42 and column 13, lines 21-23.

As per claim 3, inherently, the processor core 16 can write (i.e. configure) the internal memory and then read the data written to the internal memory at a later time, during normal microcontroller operations.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Russell (6,212,625) teaches a system on a chip including a programmable state engine.

10. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 305-9051, (for formal communications intended for entry)

Or:

(703) 305-9731 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (703) 305-3823. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Matthew Kim, can be reached at (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2185

RGB
11-Feb-01